an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor; and

a first interconnection layer formed on the interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the distance between the top electrode and another top electrode adjacent to the top electrode is smaller than the width of a bit line formed above the top electrode.

2. (Amended) The device of Claim 1, wherein the first interconnection layer includes:

a storage line connected to the top electrode of the ferroelectric capacitor and to the first doped layer of the memory cell transistor, the storage line having a linear planar pattern; and

[a] the bit line connected to the second doped layer of the memory cell transistor, and

wherein the storage line intersects only one side of the top electrode in the planar layout.

REMARKS

The Official Action of January 13, 2000 was received and carefully reviewed. Claims 1-10 are currently pending in this application. Reconsideration and allowance of the present application are respectfully requested.

On page 2 of the Official Action, claims 2 and 6, and claims 8 and 9 are objected to as containing identical limitations. Applicants respectfully traverse this objection for the reasons provided below.

Applicants respectfully submit that dependent claim 2 is directed to overlapping of the storage line 20 with the top electrode 18. On the other hand, claim 6 recites overlapping of the bit line DBL with the top electrode 18. Thus, Applicants submit that claims 2 and 6 differ in scope. See, for example, Figures 1 and 2. Additionally, Applicants submit that dependent claim 8 is directed to overlapping of a second interconnection layer with the top electrode 18 in which the second interconnection layer is formed on the upper interlevel dielectric film over the first

interconnection layer. On the other hand, claim 9 is directed to overlapping of the second interconnection layer with a bottom electrode 16. Thus, Applicants submit that claims 8 and 9 differ in scope. See, for example, Figures 1 and 2. As such, Applicants respectfully request reconsideration and withdrawal of the objection to the claims.

Also, on page 2 of the Official Action, claims 1-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' Admitted Prior Art in view of U.S. Patent No. 5,869,859 to Hanagasaki. Applicants respectfully traverse this rejection for the reasons provided below.

Independent claim 1 recites a nonvolatile semiconductor memory device with a ferroelectric capacitor in which first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, not covering at least one side of the rectangular top electrode, so as to eliminate deterioration in characteristics of the ferroelectric capacitor.

The Applicants' Prior Art (hereinafter APA) teaches a nonvolatile semiconductor memory device with a ferroelectric capacitor in which a first interconnection layer forming a storage line overlaps with the top electrode of the ferroelectric capacitor, and covers two opposite sides of the rectangular top electrode. The APA further teaches that, in a planar layout, a bit line crosses at right angle with two opposite sides of the rectangular top electrode and overlaps with the top electrode, covering the two opposite sides of the top electrode.

The presently claimed invention, as recited in claims 1-10, is different from the APA because the present invention teaches a first interconnection layer that overlaps with a top electrode and does not cover at least one side of the rectangular top electrode of the capacitor, while the APA teaches that the storage line and the bit line overlap with the top electrode of the capacitor and covers all the four sides of the rectangular top electrode.

Hanagasaki, used to solve the deficiencies of the APA, discloses a DRAM memory cell with a dielectric capacitor in which the capacitor is formed on a field oxide film, and a silicon nitride film having a high dielectric constant is used as a capacitor dielectric layer. A gate insulating film of a transistor and part of a capacitor dielectric layer of the capacitor are formed at the same time, and the gate electrode of the transistor and an upper capacitor electrode of the capacitor are formed at

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the same time. The object of Hanagasaki is to lessen the process load and to reduce the cell size of a memory.

The presently claimed invention is distinguished over Hanagasaki for the following reasons. First, as shown in Figure 1, Hanagasaki discloses a structure in which an interconnection 11 connecting a drain region 9b of the transistor and an upper electrode 8b of the capacitor overlaps with the upper electrode 8b, covering one side of the upper electrode 8b. Next, as is clear from Figure 3, Hanagasaki fails to disclose interconnections between upper electrodes to the capacitor, between C1 and C2 adjacent to each other, and between C2 and C3 adjacent to each other. On the other hand, the presently claimed invention, as illustrated in Figures 1 and 2, discloses not only that a storage line 20 connecting a doped layer 13 of the memory cell transistor and a top electrode 18, partially overlaps the top electrode 18 covering part of the top electrode 18, but also that the width of a bit line DB connected to the doped layer 13 of the memory cell is smaller than the distance between the top electrode 18 and another adjacent top electrode.

Thus, Applicants submit that Hanagasaki fails to teach the arrangement of the bit line of the presently claimed invention. Even if Hanagasaki is combined with the APA, it is impossible to achieve the device of the present invention. Applicants submit that if Hanagasaki is applied to the APA, it is possible to obtain the structure in which the storage line 60 connecting source/drain doped layers 53 and the a top electrode 58 overlaps with the top electrode 58, covering one side of the top electrode 58. However, because Hanagasaki fails to disclose any line above the upper electrode, it is impossible to obtain that the distance between two electrodes of the ferroelectric capacitor which are adjacent to each other is larger than the width of the bit line formed above the upper electrode, as now recited in independent claim 1. Accordingly, Applicants submit that claims 1-10, as amended, are not obvious over Hanagasaki, even in combination with the APA.

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In view of the above, claims 1-10 are believed to be in condition for allowance. Should the Examiner deem that any further action by the Applicant would be desirable to place this case in even better condition for issue, he is requested to contact the undersigned.

Respectfully submitted,

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